Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **OUTPUT**
2. **OUTPUT**
3. **NC**
4. **NC**
5. **INPUT**
6. **GND**

**.093”**

**2 1 6**

**5**

**3**

**4**

**DIE ID**

**1**

**4**

**0**

**F 5**

**.059”**

**NOTE: For 3 pin applications connect Vout(SENSE) to Vout**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .007” X .0076” min.**

**Backside Potential: GND**

**Mask Ref: 140F 5**

**APPROVED BY: DK DIE SIZE .059” X .093” DATE: 11/2/21**

**MFG: NATIONAL THICKNESS .013” P/N: LM140KG-5 MD8**

**DG 10.1.2**

#### Rev B, 7/19/02